UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,235	03/30/2001	Hong Wang	10559-401001 / P10338	6323

20985 7590 06/23/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,235	WANG ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, and 5-40 have been examined.

Papers Received

2. Receipt is acknowledged of Amendment papers submitted, where the papers have been placed of record in the file.

3. No arguments or amendments have been entered in regard to the objections to the specification, title, and drawings and thus the objections to these items remain as stated below.

Specification

4. The abstract of the disclosure is objected to because the acronym DAG is used without any definition of the term. The abstract must be understood when it stands alone. Correction is required. See MPEP § 608.01(b).

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Trace Cache of the Form of a Directed Acyclic Graph and Method of Constructing Such.

Drawings

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 414. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the

Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 8-14, 22, 33, 36, and 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 8 recites the limitation "the trace" in line 3 of the claim and "the information" in line 2. There is insufficient antecedent basis for these limitations in the claim. A trace has not been defined in the claims, but only trace information and likewise information has not been defined, but only trace information. The examiner is taking the claim to mean "the trace information" in both instances as it is believed that this terms were mistakenly unchanged to "trace information" since the rest of the citations of "trace" and "information" in the previous claims were changed as such.

10. Claim 11 recites the limitation "the trace" in line 4 of the claim and "the information" in line 2. There is insufficient antecedent basis for these limitations in the claim. A trace has not been defined in the claims, but only trace information and likewise information has not been defined, but only trace information. The examiner is taking the claim to mean "the trace information" in both instances as it is believed that this terms were mistakenly unchanged to "trace information" since the rest of the citations of "trace" and "information" in the previous claims were changed as such.

11. Claim 12 recites the limitation "the trace" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. A trace has not been defined in the claims, but only trace information. The examiner is taking the claim to mean "the trace information" as it is believed that this term was mistakenly unchanged to "trace information" since the rest of the citations of "trace" and "information" in the previous claims were changed as such.

12. Claim 13 recites the limitation "the trace" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. A trace has not been defined in the claims, but only trace information. The examiner is taking the claim to mean "the trace information" as it is believed that this term was mistakenly unchanged to "trace information" since the rest of the citations of "trace" and "information" in the previous claims were changed as such.

13. Claim 14 recites the limitation "the trace" in lines 3 and 4 of the claim. There is insufficient antecedent basis for this limitation in the claim. A trace has not been defined in the claims, but only trace information. The examiner is taking the claim to mean "the trace information" as it is believed that this term was mistakenly unchanged to "trace information" since the rest of the citations of "trace" and "information" in the previous claims were changed as such.

14. The term "long latency" in claim 22 is a relative term which renders the claim indefinite. The term "long latency" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner is

taking the term "long latency" to mean a longer latency than that of the predetermined time threshold of the claim as implied therein and stated in the specification.

15. The term "relatively long latencies" in claim 33 is a relative term which renders the claim indefinite. The term "relatively long latencies" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner is taking the term to mean relatively long latencies with respect to instructions that take only one clock cycle, and thus the criterion instruction has a latency greater than one clock cycle.

16. The term "relatively long latencies" in claim 36 is a relative term which renders the claim indefinite. The term "relatively long latencies" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner is taking the term to mean relatively long latencies with respect to instructions that take only one clock cycle, and thus the criterion instruction has a latency greater than one clock cycle.

17. The term "relatively long latencies" in claim 39 is a relative term which renders the claim indefinite. The term "relatively long latencies" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner is taking the term to mean relatively long latencies with respect

to instructions that take only one clock cycle, and thus the criterion instruction has a latency greater than one clock cycle.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. Claims 1-3, 5-10, 16-18, and 20-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Nair et al (Exploiting Instruction level Parallelism in Processors by Caching Scheduled Groups).

20. In regard to claim 1, Nair discloses an apparatus comprising:

a. a cache of trace information including interdependent instructions which interdependent instructions include at least an associated instruction and a criterion instruction that is part of a program sequence and which is data dependent on said associated instruction; Figure 1 shows the use of a DIF cache and the paragraph above the figure shows that this cache stores reformatted or translated sequences of previously executed instructions and is thus a trace cache based on the definition known in the art. Further proof is as follows: Figure 2 illustrates a trace of instructions. Figure 7 illustrates the trace of figure 2 after translation or reformatting and thus as stored in the cache or trace cache. The specification defines a criterion instruction in the replacement paragraph (for the paragraph beginning on page 4, line 18) on page 3 of the amendment to be a

branch or a load that can incur long latency when executed. The cached instructions of figure 7 include a criterion instruction as the second "lwz" (load) instruction of slot 3. This criterion instruction is data dependent on an associated instruction in the lwz instruction of slot 2, which is an associated instruction because of the data dependency. This criterion instruction has a source (R6.2, a register) that is the same as the destination of the associated instruction (R6.2) and thus is data dependent. As shown in figure 7, these instructions are a part of an instruction sequence including other interdependent instructions.

b. And a processor that associates first information from the associated instruction with said criterion instruction to form said trace information. As shown above, the processor reformats or translates the instructions and forms the trace stored in the cache and thus associates the criterion instruction with the associated instruction.

21. In regard to claim 2, Nair discloses the apparatus of claim 1 wherein the trace information comprises a directed acyclic graph. Figure 4, shows the dependency information included with the trace (sine the dependencies are based on the dependent operands such as in figure 2) that directly causes the scheduling shown in figure 7. This figure 4 shows that the information in each trace comprises a directed acyclic graph because the trace comprises instructions with a line between other instructions showing the dependency (sequential dependency) between them and not returning to the starting instruction, which meets the definition set forth in the specification on page 5, line 24 – page 6, line14.

22. In regard to claim 3, Nair discloses the apparatus of claim 1 wherein the trace information includes pointers to the interdependent instructions. Section 2.5 and the figures therein shows that the instructions are placed in slots for execution to be executed as soon as possible and that the program counter stays fixed on the first instruction in the sequence comprising the group or trace. Therefore, it is inherent that the instruction slots (which are included with the trace information as shown in figure 7) include pointers to the next slot to execute the instructions held there.

23. In regard to claim 5, Nair discloses the apparatus of claim 1 wherein the interdependent instructions include the criterion instruction and instructions preceding the criterion instruction in the program sequence, as shown in figure 7.

24. In regard to claim 6, Nair discloses the apparatus of claim 1 wherein the interdependent instructions are classified into subslice types, the trace information including a pointer to each subslice that is formed by each type of the interdependent instructions. Figure 7 shows how the instructions are divided and classified into different slots or subslice types. Section 2.5 and the figures therein shows that the instructions are placed in slots for execution to be executed as soon as possible and that the program counter stays fixed on the first instruction in the sequence comprising the group or trace. Therefore, it is inherent that the instruction slots (which are included with the trace information as shown in figure 7) include pointers to the next slot to execute the instructions held there.

25. In regard to claim 7, Nair discloses the apparatus of claim 6 wherein each subslice is stored as dependent pieces. Figure 7 shows that there are dependencies between instructions in different slots as described above.

26. In regard to claim 8, Nair discloses the apparatus of claim 1 wherein the trace information includes a triggering condition of the trace information, the interdependent instructions of the trace information being executed when the triggering condition is met. Section 2.5 shows that "greedy" scheduling is used, which means that instructions are placed in an appropriate slot in the trace according to the earliest time they can be executed. This section then shows that the registers have slot fields that indicate when data in the registers is ready for use by instructions. This means that the slot in the trace information is a condition, waiting for register data to become available. When the slot in the register indicates ready, the condition is met and execution is triggered for the interdependent instructions therein.

27. In regard to claim 9, Nair discloses the apparatus of claim 8 wherein the triggering condition includes a triggering instruction in the program sequence, the triggering condition being based on evaluation of an architectural state. The triggering condition is based on the state of the general-purpose architectural register, ready or not ready. The register is ready when all writes to the register are accomplished so correct data is used. These writes are inherently accomplished by instructions and thus are triggering instructions since they indirectly specify when the register is ready for another slot of instructions.

28. In regard to claim 10, Nair discloses the apparatus of claim 8 wherein the triggering condition includes a triggering instruction in the program sequence, the triggering condition being based on evaluation of a micro-architectural state. The triggering condition is based on the state of the general-purpose architectural register, ready or not ready. When microinstructions are executed and manipulate these registers they are then micro-architectural registers. The register is ready when all writes to the register are accomplished so correct data is used. These writes are inherently accomplished by instructions and thus are triggering instructions since they indirectly specify when the register is ready for another slot of instructions. The second paragraph of section 2.2 shows that microcode is used since complex instructions are broken up into simpler ones, which is the definition of such microcode or microinstructions.

29. In regard to claim 16, Nair discloses the apparatus of claim 1 wherein traces that are data dependent of each other are chained together for serial executions. Section 2.6 shows that a group (the trace of figure 7) is closed or terminated under certain conditions. This means that another trace inherently must begin filling unless the processor halts. Since the trace itself takes full advantage of parallel execution as shown in section 2.4, there is no choice but to execute the next trace in serial, dependent or not.

30. In regard to claim 17, Nair discloses the apparatus of claim 1 further comprising an instruction pointer that indexes the trace information, the instruction pointer pointing to a first instruction or a last instruction of the interdependent instructions. The second

paragraph before section 2.5.1 on page 19 states that a program counter (instruction pointer) remains pointed to the first instruction in the sequence as it executes.

31. In regard to claim 18, Nair discloses the apparatus of claim 1 further comprising: a main pipeline executing the program sequence; and at least one secondary pipeline disjoint from the main pipeline executing the interdependent instructions. Figure 1 shows that there are two pipelines or engines, a primary (main) and a parallel (secondary). The primary engine determines the cacheable sequences of instructions to be scheduled by the translator, executes certain special instructions in the program sequence, and is used sparingly as a safety net. In addition, the first paragraph of page 14 shows that the primary engine initially executes the program sequence. The parallel engine implements the rest of the code, as shown in both these sections, which entails the trace execution of interdependent instructions.

32. In regard to claim 20, Nair discloses a method comprising:

a. identifying a criterion instruction incurring latency in a program sequence; The specification defines a criterion instruction in the replacement paragraph (for the paragraph beginning on page 4, line 18) on page 3 of the amendment to be a branch or a load that can incur long latency when executed. The program sequence of figure 7 includes a criterion instruction as the second "lwz" (load) instruction of slot 3. These instructions inherently have latency as all instructions take cycle time to complete.

b. capturing the criterion instruction and instructions preceding the criterion instruction in the program sequence, the preceding instructions and the criterion

instruction being interdependent; The criterion instruction and preceding instructions are captured as shown in figure 7. This criterion instruction is data dependent on an lwz instruction of slot 2. This criterion instruction has a source (R6.2, a register) that is the same as the destination of the associated instruction (R6.2) and thus is data dependent. The criterion instruction is also indirectly data dependent on the addic instruction of slot 1 since the lwz of slot 2 is dependent on this addic instruction due to a read after write hazard involving the register R26.1. Thus the criterion instruction is interdependent on multiple preceding instructions

c. storing additional instructions relating to said criterion instruction; Figure 7 shows many additional instructions related to the criterion instruction in that they are in the same trace as defined below.

d. and storing a trace in a trace cache, the trace including information about the criterion instruction interpreted according to said additional instructions and the preceding instructions. Figure 1 shows the use of a DIF cache and the paragraph above the figure shows that this cache stores reformatted or translated sequences of previously executed instructions and is thus a trace cache based on the definition known in the art. Further proof is as follows: Figure 2 illustrates a trace of instructions. Figure 7 illustrates the trace of figure 2 after translation or reformatting and thus as stored in the cache or trace cache. The criterion instruction is interpreted according to the preceding instructions in that it is dependent on them as shown above and data dependencies must be

resolved in order for dependent instructions to execute. The additional instructions include the first lwz instruction of slot 0. The addic instruction is data dependent on this instructions for the same reasons as illustrated for the other dependencies above and therefore the criterion instruction, which is indirectly dependent on the addic instruction is also indirectly dependent on the lwz and interpreted according to this additional instruction. The stw instruction of slot 4 is dependent on the criterion instruction due to a write to the same register R27.1 and thus the criterion instruction is interpreted according to this additional instruction as well.

33. In regard to claim 21, Nair discloses the method of claim 20 wherein the information is in a form of a directed acyclic graph. Figure 4, shows the dependency information included with the trace (sine the dependencies are based on the dependent operands such as in figure 2) that directly causes the scheduling shown in figure 7. This figure 4 shows that the information in each trace comprises a directed acyclic graph because the trace comprises instructions with a line between other instructions showing the dependency (sequential dependency) between them and not returning to the starting instruction, which meets the definition set forth in the specification on page 5, line 24 – page 6, line14.

34. In regard to claim 22, Nair discloses the method of claim 20 wherein the latency includes a long latency that exceeds a predetermined time threshold, a frequent latency that exceeds a predetermined recurrence threshold, or a long and uncertain latency that exceeds a mean threshold and a variance threshold. Since there is no claimed purpose

of this threshold or what the threshold may be, the examiner is taking the threshold to be 0 cycles, a predetermined time threshold. In such a case, the criterion instruction exceeds this threshold since an instruction must have latency and thus the latency includes a long latency.

35. In regard to claim 23, Nair discloses the method of claim 20 further comprising dynamically identifying the criterion instruction based on information derived from previous executions. As shown on page 14, first paragraph, the instructions are reformatted according to an execution previous to the reformatted execution. As shown above, in section 2.3, and in figures 2, 6 and 7, the criterion instruction is identified and it's dependencies are managed for optimal execution based on this reformatting or translating of the previous execution.

36. In regard to claim 24, Nair discloses the method of claim 20 further comprising capturing the criterion instruction and the preceding instructions by a buffer. As shown above, the criterion and preceding instructions are stored or captured in a trace cache. The included IEEE dictionary definitions for the term "buffer" show that a buffer is a temporary storage device for holding data to be transferred to another device. The trace cache holds the required instruction data and sends it to appropriate execution devices with in the processor as discussed above and shown in figure 10 and thus the trace cache is a buffer that captures the criterion and preceding instructions.

37. In regard to claim 25, Nair discloses the method of claim 20 further comprising locating an existing trace in the trace cache before storing the trace, the existing trace and the trace to be stored having the same first instruction or the same last instruction.

The paragraph of above the code segment on page 20 shows an embodiment where when instructions are attempting to fill a trace (group), or store a trace of new instructions, first it is seen if an instruction is already the starting instruction of an existing trace in the cache.

38. In regard to claim 26, Nair discloses the method of claim 20 further comprising rebuilding the trace after a duration of time interval that grows each time the trace is rebuilt until the duration reaches a predetermined time limit. The first few paragraphs of section 2.6, show that a trace is terminated is if it reaches a predetermined maximum of various resources. If this maximum is not reached, then the trace continues to be filled, or rebuilt. It is inherent that as a trace grows, just like an array, every time it is rebuilt, the time it takes to do so is longer. Therefore, the maximum set size given is associated with a maximum (predetermined) time limit.

39. In regard to claim 27, Nair discloses the method of claim 20 further comprising storing, in an array, the information about the criterion instruction and the preceding instructions. The include IEEE dictionary definitions show that an "array" is a group of memory cells arranged in a pattern, as it applies to hardware. Figure 7 shows that the criterion instruction and preceding instructions (and thus information about them) are stored in a multiple slots or memory cells (as shown in figures 12 and 13) arranged in the given pattern and thus are stored in an array.

40. In regard to claim 28, Nair discloses the method of claim 27 wherein the array further includes a subslice type for each of the instructions, the subslice type being a result of classifying the instructions. Figure 7 shows how the instructions are divided

and classified into different slots or subslice types based on dependency classifications as shown in section 2.3.

41. In regard to claim 29, Nair discloses a computer program residing on a computer readable medium caused to:

a. identify a criterion instruction incurring latency in a program sequence; The specification defines a criterion instruction in the replacement paragraph (for the paragraph beginning on page 4, line 18) on page 3 of the amendment to be a branch or a load that can incur long latency when executed. The program sequence of figure 7 includes a criterion instruction as the second "lwz" (load) instruction of slot 3. These instructions inherently have latency as all instructions take cycle time to complete.

b. capture the criterion instruction and instructions preceding the criterion instruction in the program sequence, the preceding instructions and the criterion instruction being interdependent; The criterion instruction and preceding instructions are captured as shown in figure 7. This criterion instruction is data dependent on an lwz instruction of slot 2. This criterion instruction has a source (R6.2, a register) that is the same as the destination of the associated instruction (R6.2) and thus is data dependent. The criterion instruction is also indirectly data dependent on the addic instruction of slot 1 since the lwz of slot 2 is dependent on this addic instruction due to a read after write hazard involving the register R26.1. Thus the criterion instruction is interdependent on multiple preceding instructions

c. Storing additional instructions relating to said criterion instruction; Figure 7 shows many additional instructions related to the criterion instruction in that they are in the same trace as defined below.

d. and store a trace in a trace file, the trace including information about the criterion instruction interpreted according to said additional instructions, the preceding instructions, and interdependency among the criterion instruction and the preceding instructions. As shown above, the trace is stored in a trace cache. By storing the criterion and preceding instructions, the trace includes information about these instructions. Figure 1 shows the use of a DIF cache and the paragraph above the figure shows that this cache stores reformatted or translated sequences of previously executed instructions and is thus a trace cache based on the definition known in the art. Further proof is as follows: Figure 2 illustrates a trace of instructions. Figure 7 illustrates the trace of figure 2 after translation or reformatting and thus as stored in the cache or trace cache. The criterion instruction is interpreted according to the preceding instructions in that it is dependent on them as shown above and data dependencies must be resolved in order for dependent instructions to execute. The additional instructions include the first lwz instruction of slot 0. The addic instruction is data dependent on this instructions for the same reasons as illustrated for the other dependencies above and therefore the criterion instruction, which is indirectly dependent on the addic instruction is also indirectly dependent on the lwz and interpreted according to this additional instruction. The stw instruction of slot 4 is

dependent on the criterion instruction due to a write to the same register R27.1 and thus the criterion instruction is interpreted according to this additional instruction as well.

As shown throughout the disclosure of Nair, the operation of the computer is all caused by instructions (of a computer program) and how they are scheduled and executed.

42. In regard to claim 30, Nair discloses the computer program of claim 29 wherein an analysis window defined in the computer program causes the computer to capture the criterion instruction and preceding instructions. As shown in figure 7, the criterion and preceding instructions are captured as a trace based on the trace of figure 2, an analysis window that is then translated into the arrangement of figure 7.

43. In regard to claim 31, Nair discloses the computer program of claim 29 wherein the computer identifies the criterion instruction by profiling the program sequence. The examiner is taking profiling to mean outlining or organizing as is consistent with the common dictionary definition since there is no definition in the specification. Therefore, since the trace of figure 2 is scanned before reformatting for dependencies, the criterion must be identified so the program sequence of the trace of figure 7 may be organized and thus the criterion instruction is identified during this profiling of the program sequence.

44. In regard to claim 32, Nair discloses the apparatus of claim 1, wherein there are multiple associated instructions associated with said criterion instruction, and said processor forms first trace information using a first of said associated instructions, and second trace information using a second of said associated instructions. Figure 7

shows that the criterion instruction is data dependent on an lwz instruction of slot 2. This criterion instruction has a source (R6.2, a register) that is the same as the destination of the associated instruction (R6.2) and thus is data dependent and first information regarding this first instruction and its dependency has been formed. The criterion instruction is also indirectly data dependent on the addic instruction of slot 1 since the lwz of slot 2 is dependent on this addic instruction due to a read after write hazard involving the register R26.1 and thus second trace information has been formed based on this second instruction and its dependency.

45. In regard to claim 33, Nair discloses the apparatus as in claim 1, wherein said criterion instructions are instructions which represent relatively long latencies in execution. The criterion instruction illustrated above is a load. It is inherent that if a load misses the cache, it will take longer than one cycle to fetch from memory.

46. In regard to claim 34, Nair discloses the apparatus as in claim 1, wherein the criterion instructions include template data for an instruction form, and the associated instructions include information that assigns values of register information within the criterion instructions. It is inherent that the criterion instruction has a given format or template so that the processor recognizes it and knows how to handle it. Since the criterion instruction is data dependent on other instructions as shown in figure 7, When the data the criterion instruction needs to read is updated by the associated instructions (lwz of slot 2, addic of slot 1), these associated instructions are assigning values of register information that is used within the criterion instruction when it executes.

47. In regard to claim 35, Nair discloses the method as in claim 20, further comprising associating multiple different associated instructions with said criterion instruction, and said storing comprising forms first trace information using a first of said associated instruction and second trace information using a second set of said associated instructions. Figure 7 shows that the criterion instruction is data dependent on an lwz instruction of slot 2. This criterion instruction has a source (R6.2, a register) that is the same as the destination of the associated instruction (R6.2) and thus is data dependent and first information regarding this first instruction and its dependency has been formed. The criterion instruction is also indirectly data dependent on the addic instruction of slot 1 since the lwz of slot 2 is dependent on this addic instruction due to a read after write hazard involving the register R26.1 and thus second trace information has been formed based on this second instruction and its dependency.

48. In regard to claim 36, Nair discloses the apparatus as in claim 20, wherein said criterion instructions are instructions which represent relatively long latencies in execution. The criterion instruction illustrated above is a load. It is inherent that if a load misses the cache, it will take longer than one cycle to fetch from memory.

49. In regard to claim 37, Nair discloses the apparatus as in claim 20, wherein the criterion instructions include template data for an instruction form, and the associated instructions include information that assigns values of register information within the criterion instructions. It is inherent that the criterion instruction has a given format or template so that the processor recognizes it and knows how to handle it. Since the criterion instruction is data dependent on other instructions as shown in figure 7, When

the data the criterion instruction needs to read is updated by the associated instructions (lwz of slot 2, addic of slot 1), these associated instructions are assigning values of register information that is used within the criterion instruction when it executes.

50. In regard to claim 38, Nair discloses the method as in claim 29, further comprising associating multiple different associated instructions with said criterion instruction, and said storing comprising forms first trace information using a first of said associated instruction and second trace information using a second set of said associated instructions. Figure 7 shows that the criterion instruction is data dependent on an lwz instruction of slot 2. This criterion instruction has a source (R6.2, a register) that is the same as the destination of the associated instruction (R6.2) and thus is data dependent and first information regarding this first instruction and its dependency has been formed. The criterion instruction is also indirectly data dependent on the addic instruction of slot 1 since the lwz of slot 2 is dependent on this addic instruction due to a read after write hazard involving the register R26.1 and thus second trace information has been formed based on this second instruction and its dependency.

51. In regard to claim 39, Nair discloses the apparatus as in claim 29, wherein said criterion instructions are instructions which represent relatively long latencies in execution. The criterion instruction illustrated above is a load. It is inherent that if a load misses the cache, it will take longer than one cycle to fetch from memory.

52. In regard to claim 40, Nair discloses the apparatus as in claim 29, wherein the criterion instructions include template data for an instruction form, and the associated instructions include information that assigns values of register information within the

criterion instructions. It is inherent that the criterion instruction has a given format or template so that the processor recognizes it and knows how to handle it. Since the criterion instruction is data dependent on other instructions as shown in figure 7, When the data the criterion instruction needs to read is updated by the associated instructions (lwz of slot 2, addic of slot 1), these associated instructions are assigning values of register information that is used within the criterion instruction when it executes.

Claim Rejections - 35 USC § 103

53. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

54. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair in view of Killian (6,092,187).

55. In regard to claim 11,

a. Nair discloses the apparatus of claim 1.

b. Nair does not disclose wherein the information further includes a confidence metric of the trace information that predicts the likelihood of producing a correct result from executing the trace information.

c. Killian has shown in column 5, lines 32-36, that a trace cache uses confidence levels (metrics). These confidence levels predict the likelihood of producing a correct prediction as shown in column 3, lines 59-65. Killian shows

in lines 64-65 that a larger confidence value yields greater confidence in a prediction.

d. It is well known in the art that greater confidence in a prediction is desirable. This greater confidence would have motivated one of ordinary skill in the art to modify the design of Nair to use the confidence levels taught by Killian. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Nair to include the confidence level system taught by Killian so that greater confidence in the instruction predictions of traces can be realized.

56. In regard to claim 12, Nair in view of Killian discloses the apparatus of claim 11 wherein the confidence metric of the trace indicates whether or not the trace should be replaced by a new trace storing information about different instructions. The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the trace cache is controlled by the confidence levels and predictions are made by the traces, if the predictor is changed, that means the trace and all its instructions are replaced with new ones.

57. In regard to claim 13, Nair in view of Killian discloses the apparatus of claim 11 wherein the confidence metric of the trace indicates whether or not the trace should be rebuilt using new information about the criterion instruction that arrives at the trace cache. The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the trace cache is controlled by the confidence levels and predictions are made

by the traces, if the predictor is changed, that means the trace and all its instructions are replaced with new ones. Thus the trace that is sent for execution must be replaced or rebuilt. Since all traces use information from the criterion instruction to know where the trace ends. The trace is rebuilt using information from this criterion instruction.

58. In regard to claim 14, Nair in view of Killian discloses the apparatus the apparatus of claim 11 further comprising a counter having a counter value that indicates the number of times the trace has been executed, the counter value, when exceeding a frequency threshold of the trace, triggering the trace to be rebuilt. Column 15, lines 56-59 of Killian show the use of counters for prediction as taught in the background. Here in column 3, lines 59-67, it is shown that a suggested confidence level measure is using a counter to keep track of the number of executions of the trace without a misprediction. The threshold here is zero. When a misprediction is encountered the counter is reset to zero and the more correct predictions the higher the confidence level. The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the trace cache is controlled by the confidence levels and predictions are made by the traces, if the predictor is changed, that means the trace and all its instructions are replaced with new ones. With the confidence level surpassing the threshold at zero, there is no confidence and a different predictor (trace) will be selected or rebuilt for execution.

59. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nair in view of Ferreira de Souza (Dynamically Scheduling the Trace Produced During Program Execution into VLIW Instructions)

60. In regard to claim 15,

a. Nair discloses the apparatus of claim 1

b. Nair does not disclose wherein traces that are independent of each other and adjacent in the program sequence are grouped into a very-long-instruction-word for parallel executions. Nair instead discloses a single trace of instructions (figure 2) that can be represented as a single VLIW instruction (first paragraph of section 2.1).

c. Ferreira de Souza discloses in section 1 that all traces are scheduled into VLIW (very-long-instruction-word) instructions for execution. This means that traces independent of each other in the program sequence are grouped into VLIW instructions. Since it is also shown here that VLIW machines execute operations in parallel.

d. The introduction section of Ferreira de Souza also shows that by converting these traces into VLIW instructions, VLIW performance and simplicity is attained. This performance and simplicity would have motivated one of ordinary skill in the art to modify the design of Nair to group traces into VLIW instructions as taught by Ferreira de Souza.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Nair to group traces into VLIW instructions as taught by Ferreira de Souza to increase performance and simplicity.

61. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nair in view of Tullsen et al (Simultaneous Multithreading: Maximizing On-Chip Parallelism).

62. In regard to claim 19,

a. Nair discloses the apparatus of claim 1 wherein the interdependent instructions are executed by a secondary thread on a pipeline, and the program sequence is executed by a main thread on a pipeline. Figure 1 shows that there are two pipelines or engines, a primary (main) and a parallel (secondary). The primary engine determines the cacheable sequences of instructions to be scheduled by the translator, executes certain special instructions in the program sequence, and is used sparingly as a safety net. In addition, the first paragraph of page 14 shows that the primary engine initially executes the program sequence. The parallel engine implements the rest of the code, as shown in both these sections, which entails the trace execution of interdependent instructions.

b. Nair does not disclose that the two threads are on the same pipeline.

c. Tullsen has taught a simultaneous multithreading implementation, throughout the disclosure, which entails executing multiple threads in parallel on a single pipeline.

d. The first paragraph of section 6 shows that the SM (simultaneous multithreading) processor requires fewer resources relative to multiprocessing, in order to achieve the same desired level of performance. The ability to use fewer resources while not sacrificing performance would have motivated one of ordinary skill in the art at the time of invention to modify the design of Nair to use simultaneous multithreading as taught by Tullsen.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Nair to use the simultaneous multithreading technique taught by Tullsen for the two processing engines so that fewer system resources are used while not sacrificing performance.

Response to Arguments

63. The examiner would first like to point out that the claims mentioned in the second paragraph of page 16 of the amendment as being rejected under 35 USC 102(b) as being unpatentable over Peled were actually rejected under 35 USC *102(e)* as being *anticipated* by Peled.

64. The examiner would like to point out that page 16 of the arguments states that, "Claim 24 has been cancelled and new claim 32 is substituted herein," however the listing of amended claims makes no indication of claim 24 being cancelled. The examiner is disregarding the statement of page 16 and taking the claim listing of pages 5-15 to be accurate.

65. Applicant's arguments with respect to claims 1-3 and 5-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

66. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

67. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

68. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited in the previous action remain pertinent and are cited herein as well.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
June 16, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100